WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a plurality of synchronous modules, each synchronous module having an associated clock domain characterized by a data rate, the data rates comprising a plurality of different data rates;

a plurality of clock domain converters, each clock domain converter being coupled to a corresponding one of the synchronous modules, and being operable to convert data between the clock domain of the corresponding synchronous module and an asynchronous domain characterized by transmission of data according to an asynchronous handshake protocol; and

an asynchronous crossbar coupled to the plurality of clock domain converters, and operable in the asynchronous domain to implement a first-in-first-out (FIFO) channel between any two of the clock domain converters, thereby facilitating communication between any two of the synchronous modules.

2. The integrated circuit of claim 1 wherein each clock domain converter comprises a datapath operable to transfer a data token between the corresponding clock domain and the asynchronous domain, each clock domain converter further comprising control circuitry operable to enable transfer of the data token via the datapath in response to at least one transition of a clock signal associated with the corresponding clock domain and at least one completion of the asynchronous handshake protocol.

3. The integrated circuit of claim 2 wherein the datapath of each clock domain converter is operable to transfer the data token from the asynchronous domain to the

corresponding clock domain, and the at least one completion of the asynchronous handshake protocol corresponds to receipt of the data token.

4. The integrated circuit of claim 3 wherein the data token comprises one of parallel and serial data.

5. The integrated circuit of claim 3 wherein a particular one of the clock domains requires a data transfer to comprise a block of consecutive data, the datapath of the corresponding clock domain converter further being operable to accumulate data tokens generated in the asynchronous domain to form the block of consecutive data, and wherein the control circuitry of the corresponding clock domain converter is operable to facilitate transfer of the accumulated data tokens to the particular clock domain via the corresponding datapath in response to a synchronous handshake with the particular clock domain and consecutive transitions of the clock signal, and after completion of the asynchronous handshake protocol for the data token.

6. The integrated circuit of claim 2 wherein the datapath of each clock domain converter is operable to transfer the data token from the corresponding clock domain to the asynchronous domain, and the at least one completion of the asynchronous handshake protocol corresponds to a previously transferred data token.

7. The integrated circuit of claim 6 wherein each of the data token and the previously transferred data token comprises one of parallel and serial data.

8. The integrated circuit of claim 6 wherein a particular one of the clock domains requires a data transfer to comprise a block of consecutive data, the control circuitry of the corresponding clock domain converter further being operable to facilitate transfer of a plurality of data tokens as the block of consecutive data to the asynchronous domain via the corresponding datapath in response to a synchronous handshake with the particular clock domain, consecutive transitions of the clock signal, and an enable signal generated in accordance with the asynchronous handshake protocol and indicating that the asynchronous domain has sufficient memory to receive the plurality of data tokens.

9. The integrated circuit of claim 2 wherein at least one of the clock domain converters is operable to transfer bursts of data tokens between the corresponding clock domain and the asynchronous domain.

10. The integrated circuit of claim 9 wherein the bursts of data tokens are variable in size.

11. The integrated circuit of claim 1 wherein the asynchronous crossbar is operable to route the data from any of a first number of input channels to any of a second number of output channels according to routing control information, each combination of an input channel and an output channel comprising one of a plurality of links, the crossbar being operable to route the data in a deterministic manner on each of the links thereby preserving a partial ordering represented by the routing control information, wherein events on different links are uncorrelated.

12. The integrated circuit of claim11 wherein the crossbar is operable to transfer the data on at least one of the links based on at least one timing assumption.

13. The integrated circuit of claim 12 wherein the at least one timing assumption comprises any of a pulse timing assumption, an interference timing assumption, and an implied-data-neutrality timing assumption.

14. The integrated circuit of claim 1 wherein the asynchronous handshake protocol between a first sender and a first receiver comprises:

the first sender sets a data signal valid when an enable signal from the first receiver goes high;

the first receiver lowers the enable signal upon receiving the valid data signal;

the first sender sets the data signal neutral upon receiving the low enable signal; and

the first receiver raises the enable signal upon receiving the neutral data signal.

15. The integrated circuit of claim 1 wherein the asynchronous handshake protocol is delay-insensitive.

16. The integrated circuit of claim 1 further comprising at least one repeater, each repeater being coupled between a selected one of the clock domain converters and the asynchronous crossbar.

17. The integrated circuit of claim 16 wherein each repeater comprises an asynchronous half-buffer circuit.

18. The integrated circuit of claim 1 wherein the asynchronous crossbar is operable to arbitrate among multiple requests corresponding to a same destination synchronous module.

19. The integrated circuit of claim 18 wherein the asynchronous crossbar comprises arbitration circuitry to effect arbitration, the arbitration circuitry comprising at least one Seitz arbiter.

20. The integrated circuit of claim 1 further comprising a rate throttling circuit associated with a specific one of the synchronous modules which is operable to control transmission of the data to the corresponding clock domain converter.

21. The integrated circuit of claim 20 wherein the rate throttling circuit is operable to control transmission of the data by delaying transmission of the data in accordance with a priority associated with the specific synchronous module.

22. The integrated circuit of claim 20 wherein the rate throttling circuit is operable to control transmission of the data in response to congestion between the corresponding clock domain converter and the asynchronous crossbar.

23. The integrated circuit of claim 22 wherein the rate throttling circuit is operable to determine the congestion with reference to the asynchronous handshake protocol between the corresponding clock domain converter and the asynchronous crossbar.

24. The integrated circuit of claim 1 further comprising a built-in-self-test (BIST) module between one of the clock domain converters and the asynchronous crossbar, the BIST module being operable to transmit test vectors to and receive result vectors from each of the synchronous modules via the asynchronous crossbar.

25. The integrated circuit of claim 24 wherein the BIST module comprises a scan register for receiving the test vectors from external test equipment.

26. The integrated circuit of claim 24 wherein the BIST module is operable to transmit a first test vector to a first one of the synchronous modules via the asynchronous crossbar, the first synchronous module being operable to transmit a first result vector corresponding to the first test vector to a second one of the synchronous modules via the asynchronous crossbar, the second synchronous module being operable to transmit a second result vector to the BIST module via the asynchronous crossbar, the BIST module being further operable to verify the second result vector.

27. The integrated circuit of claim 1 wherein the integrated circuit comprises a multi-processor system, the plurality of synchronous modules comprising at least two central processing units with associated cache memory, at least one memory controller, at least one internal peripheral device, and at least one I/O interface.

28. The integrated circuit of claim 27 further comprising at least one repeater, each repeater being coupled between a selected one of the clock domain converters and the asynchronous crossbar.

29. The integrated circuit of claim 1 wherein the integrated circuit comprises a synchronous optical network (SONET) interconnect switch, the plurality of synchronous modules comprising a plurality of SONET interfaces.

30. The integrated circuit of claim 29 further comprising at least one repeater, each repeater being coupled between a selected one of the clock domain converters and the asynchronous crossbar.

31. The integrated circuit of claim 1 wherein the integrated circuit comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit.

32. At least one computer-readable medium having data structures stored therein representative of the integrated circuit of claim 1.

33. The at least one computer-readable medium of claim 32 wherein the data structures comprise a simulatable representation of the integrated circuit.

34. The at least one computer-readable medium of claim 33 wherein the simulatable representation comprises a netlist.

35. The at least one computer-readable medium of claim 32 wherein the data structures comprise a code description of the integrated circuit.

36. The at least one computer-readable medium of claim 35 wherein the code description corresponds to a hardware description language.

37. A set of semiconductor processing masks representative of at least a portion of the integrated circuit of claim 1.